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Applicants: John W. Rapp, Larry Jackson, Mark Jones, and Troy Cherasaro

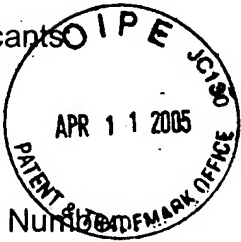
Title: PIPELINE ACCELERATOR FOR IMPROVED COMPUTING ARCHITECTURE AND RELATED SYSTEM AND METHOD

Serial Number: 10/683,929

Filing Date: October 9, 2003


Examiner/Unit: / 2818

Attorney Docket No.: 1934-13-3



CERTIFICATE OF MAILING OR TRANSMISSION

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ACCOMPANYING SECTION 1.97(e) CERTIFICATION**

TO THE COMMISSIONER FOR PATENTS:

In compliance with 37 CFR § 1.56 and § 1.97, Applicants acting by and through the attorney of record, hereby discloses patents and other documents listed on the attached Form PTO-1449 which may be considered relevant to the examination of the subject application.

Copies of the cited references are enclosed.

Certification Under Section 1.97(e)

Several items of information contained in this Information Disclosure Statement was first cited in any communication from a foreign Patent Office in a counterpart foreign application not more than three months prior to the filing of this statement.

For those items of information contained in this Information Disclosure Statement that was first cited in any communication from a foreign Patent Office in a counterpart foreign application more than three months prior to the filing of this statement, no Office Action has been mailed in this application.

Respectfully submitted,

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Substitute for form 1449A/PTO

Complete if Known

(Use as many sheets as necessary)

Sheet 1 of 2

<i>Application Number</i>	10/683,929
<i>Filing Date</i>	October 9, 2003
<i>First Named Inventor</i>	John W. Rapp
<i>Art Unit</i>	2818
<i>Examiner Name</i>	
<i>Attorney Docket Number</i>	1934-13-3

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Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³ - Number ⁴ - Kind Code ⁵ (if known)				
		EP 1 061 438 A1	12/20/00	Hewlett-Packard Company		
		EP 0 945 788 A2	09/29/99	Texas Instruments Incorporated		
		EP 0 945 788 A3	06/26/02	Texas Instruments Incorporated		
		EP 0 694 847 A2	01/31/96	International Business Machines Corporation		

**Examiner
Signature**

Date
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Sheet 2 of 2

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Application Number	10/683,929
Filing Date	October 9, 2003
First Named Inventor	John W. Rapp
Art Unit	2818
Examiner Name	
Attorney Docket Number	1934-13-3

NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		LECURIEUX-LAFAYETTE G: "Un Seul FPGA Dope Le Traitement D'Images", Electronique, CEP Communication, Paris, FR, no. 55, 1996, pp. 98, 101-103	
		VERMEULEN F. ET AL., "Flexible Hardware Acceleration for Multimedia Oriented Microprocessors", Micro-33. Proceedings of the 33 rd Annual ACM/IEEE International Symposium on Microarchitecture. Monterey, CA, Dec. 10-13, 2000, Proceedings of the Annual ACM/IEEE International Symposium on Microarchitecture, Los Alamitos, CA: IEEE Comp. Soc. US, 10 December 2000, pp. 171-177	
		International Search Report for PCT/US 03/34557, December 21, 2004	
		International Search Report for PCT/US 03/34559, January 7, 2005	

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